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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,283	04/05/2001	Kenneth J. Mobley	RAM 465	6330

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	PAPER NUMBER
2186	7

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/828,283	MOBLEY, KENNETH J.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-24 are presented for examination. This office action is in response to the amendment filed on 12/3/03.

Claim Objections

2. The objection to the claims has been withdrawn because of the amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-24 are rejected under 35 USC § 103(a) as being unpatentable over *Alwais et al, (Alwais)* U.S. Patent 5,991,851 in view of *Leung et al., (Leung)* U.S. Patent 5,394,534.

As to claim 1, *Alwais*, discloses In a memory device having plural DRAM sub-arrays (fig. 3 Refs 12s), each with plural array rows, the improvement comprising: an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request (Fig. 1 Ref. 18); and refresh circuitry, responsive to the indication of

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As to claim 1, *Alwais*, discloses In a memory device having plural DRAM sub-arrays (fig. 3 Refs 12s), each with plural array rows, the improvement comprising: an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request (Fig. 1 Ref. 18); and refresh circuitry, responsive to the indication of

the address decoder (Fig. 1 Ref. 28), wherein logically adjacent rows are placed in different sub arrays (Fig. 3 Refs. 12A & 12B, different banks reads on this limitation since last row of the first bank and the first row of the second bank are logically adjacent), however, Alwais does not specifically disclose the refresh circuitry to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory access request.

Leung discloses the refresh circuitry to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory access request (abstract lines 9-10) for the purpose of increasing access speed by preventing interference between refreshing of memory cells and accessing the memory cells externally. It is desirable in the memory art to increase access speed because it would allow to increase bandwidth and increase the system performance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the refresh circuitry to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory access request as taught by Leung into Alwais for the advantages stated above.

As to claim 2, Alwais and Leung disclose the invention as claimed above. Leung further discloses the memory access request comprises a read access request (abstract lines 9-10).

As to claim 3, Alwais and Leung disclose the invention as claimed above. Leung further discloses comprising a non-array row, external to the plural DRAM sub-arrays, for receiving from the DRAM sub-array referenced by the address of the read access request at least a portion of an array row corresponding to the address of the read access request (Fig. 1 Ref. 187).

As to claim 4, Alwais and Leung disclose the invention as claimed above. Leung further discloses the non-array row comprises an SRAM row (Fig. 1 Ref. 187).

As to claim 5, Alwais and Leung disclose the invention as claimed above. Alwais further discloses a tag register (col. 4 line 41, cache reads on this limitation since a cache stores an address (tag) and data in cache memory) for storing at least a portion of the address of a read access request that last stored information into the non-array row; and a command decoder (col. 4 lines 47-61) for signaling that the read access request may be serviced from the non-array row rather than the array row corresponding to the address of the read access request.

As to claim 6, Alwais and Leung disclose the invention as claimed above. Leung further discloses the memory access request comprises a write access request (abstract lines 9-10).

As to claim 7, Alwais and Leung disclose the invention as claimed above. Leung further discloses a non-array row, external to the plural DRAM sub-arrays, for storing (Fig. 1 Refs 185 and 187), prior to writing to the DRAM sub-array referenced by the address of the write access request, at least a portion of an array row corresponding to the address of the write access request.

As to claim 8, Alwais and Leung disclose the invention as claimed above. Alwais further discloses the refresh circuitry further comprises a refresh timer for limiting a frequency of refreshes performed (Fig. 6).

As to claim 9, Alwais and Leung disclose the invention as claimed above. Leung further discloses the refresh circuitry further comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays (col. 10 line 35 thru col. 11 line 35).

As to claim 10, Alwais and Leung disclose the invention as claimed above. Alwais further discloses the refresh circuitry (Fig. 6 Ref. 106) further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays.

As to claim 11, *Alwais* discloses a method of refreshing a memory device having plural DRAM sub-arrays (Fig. 1 Refs. 12s), each with plural array rows, the method comprising: (a) placing logically adjacent rows in different sub-arrays (Fig. 3 Refs. 12A & 12B, different banks reads on this limitation since last row of the first bank and the first row of the second bank are logically adjacent); (b) decoding an address of a memory access request (Fig. 1 Ref. 18); (c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request (Fig. 1 Ref. 18); (d) refreshing (col. 8 line 65 thru col. 9 line 12), in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request (Fig. 1 Ref. 28) and (e) executing the memory access request (abstract), however, Alwais does not specifically disclose the step of executing the memory access request, wherein steps (d) and (e) are performed contemporaneously.

Leung discloses executing the memory access request, wherein steps (d) and (e) are performed contemporaneously (abstract lines 9-10) for the purpose of increasing access speed by preventing interference between refreshing of memory

cells and accessing the memory cells externally. It is desirable in the memory art to increase access speed because it would allow to increase bandwidth and increase the system performance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate executing the memory access request, wherein steps (d) and (e) are performed contemporaneously as taught by Leung into Alwais for the advantages stated above.

As to claim 12, Alwais and Leung disclose the invention as claimed above. Leung further discloses the memory access request comprises a read access request (abstract lines 9-10).

As to claim 13, Alwais and Leung disclose the invention as claimed above. Leung further discloses receiving, into a non-array row (fig. 1 refs. 185 and 187) external to the plural DRAM sub-arrays and from the DRAM sub-array referenced by the address of the read access request, at least a portion of an array row corresponding to the address of the read access request.

As to claim 14, Alwais and Leung disclose the invention as claimed above. Leung further discloses the step of receiving comprises receiving the portion into an SRAM row (Fig. 1 Refs. 185 and 187).

As to claim 15, Alwais and Leung disclose the invention as claimed above. Alwais further discloses storing in a tag register (col. 4 line 41, cache reads on this limitation since a cache stores an address (tag) and data in cache memory) at least a portion of the address of a read access request that last stored information into the non-array row; and comparing (col. 4 lines 47-61) whether the read access request may be serviced from the non-array row rather than the array row corresponding to the address of the read access request.

As to claim 16, Alwais and Leung disclose the invention as claimed above. Leung further discloses the memory access request comprises a write access request (abstract lines 9-10).

As to claim 17, Alwais and Leung disclose the invention as claimed above. Leung further discloses storing into a non-array row (Fig. 1 Refs 185 and 187), external to the plural DRAM sub-arrays, prior to writing to the DRAM sub-array referenced by the address of the write access request, at least a portion of an array row corresponding to the address of the write access request.

As to claim 18, Alwais and Leung disclose the invention as claimed above. Alwais further discloses the refresh circuitry further comprises limiting a frequency of refreshes performed based on a refresh timer (Fig. 6).

As to claim 19, Alwais and Leung disclose the invention as claimed above. Leung further discloses tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays (col. 10 line 35 thru col. 11 line 35).

As to claim 20, Alwais and Leung disclose the invention as claimed above. Alwais further discloses updating a refresh counter to store a next array row to be refreshed in at least one of the plural DRAM sub-arrays (Fig. 6).

As to claim 21, Alwais discloses the invention as claimed. Alwais discloses a memory in a memory device (Fig. 1) having a non-array row external (Fig. 1 Ref. 14) to plural DRAM sub-arrays (Fig. 1 Refs. 12s), for receiving from the DRAM sub-array referenced by an address of an access request, the improvement comprising: a command decoder (Fig. 1 Ref. 18 and col. 9 lines 1-3) for internally determining when a refresh cycle can be hidden behind an access to the non-array row; and a controller (Fig. 1 Ref. 28) for limiting refresh cycles to a subset of possible times internally determined by the command decoder, wherein logically adjacent rows are placed in different sub arrays (Fig. 3 Refs. 12A & 12B, different banks reads on this

limitation since last row of the first bank and the first row of the second bank are logically adjacent), however, Alwais does not specifically disclose wherein at least one array row of at least one of the plural DRAM sub-arrays not referenced by the access request is refreshed while contemporaneously performing the access request.

Leung discloses at least one array row of at least one of the plural DRAM sub-arrays not referenced by the access request is refreshed while contemporaneously performing the access request (abstract lines 9-10) for the purpose of increasing access speed by preventing interference between refreshing of memory cells and accessing the memory cells externally. It is desirable in the memory art to increase access speed because it would allow to increase bandwidth and increase the system performance.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate at least one array row of at least one of the plural DRAM sub-arrays not referenced by the access request is refreshed while contemporaneously performing the access request as taught by Leung into Alwais for the advantages stated above.

As to claim 22, Alwais further discloses the non-array row comprises an SRAM row (Fig. 1 Ref. 14).

As to claim 23, Alwais further discloses the controller comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays (Fig. 6).

As to claim 24, Alwais further discloses the controller further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays (Fig.6).

Response to Arguments

Applicant's arguments filed 12/3/03 have been fully considered but they are not persuasive.

Applicant's remarks that the references not teaching at least one array row of at least one of the plural DRAM sub-arrays not referenced by the access request is refreshed while contemporaneously performing the access request and logically adjacent rows are placed in different sub arrays is not considered persuasive.

Leung discloses at least one array row of at least one of the plural DRAM sub-arrays not referenced by the access request is refreshed while contemporaneously performing the access request (abstract lines 9-10) for the purpose of increasing access speed by preventing interference between refreshing of memory cells and accessing the memory cells externally. Alwais discloses logically adjacent rows are placed in different sub arrays (Fig. 3 Refs. 12A & 12B, different banks reads on this limitation since last

row of the first bank and the first row of the second bank are logically adjacent) . Therefore broadly written claims are disclosed by the references cited.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ~~See attached PTO-892.~~

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Applicants are requested to number each line of each claim starting with line number

one to provide easier communication in the future.

When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
703-872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
February 16, 2004